IN THE CLAIMS

No amendments have been made to the claims.

1. (Previously Presented) A process, comprising:

forming a first dielectric layer on a substrate, wherein the first dielectric layer has a dielectric constant;

patterning the first dielectric layer such that a plurality of vertically oriented posts are formed on the substrate, the posts having a top surface;

forming a second dielectric layer over and adjacent to the posts, the second dielectric layer having a top surface and substantially filling up the area adjacent to said posts, wherein the second dielectric layer has a dielectric constant, said dielectric constant of the first layer being higher than said dielectric constant of the second layer;

wherein said plurality of vertically oriented posts are used to provide mechanical reinforcement of the second dielectric layer which makes up the bulk of an inter-layer dielectric material;

polishing the second dielectric layer such that its top surface is substantially even with the top surfaces of the posts; and

after forming the second dielectric layer, forming an inlaid metal interconnection in the second dielectric layer.

2. (Original) The process of Claim 1, wherein the substrate comprises a dielectric material.

3. (Original) The process of Claim 1, wherein the substrate is a material selected from the group consisting of silicon carbide, silicon nitride, and carbon doped oxides of silicon.

4. (Original) The process of Claim 1, further comprising curing the second dielectric layer.

5. (Original) The process of Claim 1, further comprising aging the second dielectric layer.

6. (Original) The process of Claim 1, further comprising forming dual damascene openings in the second dielectric layer.

7. (Original) The process of Claim 1, wherein forming the first dielectric layer comprises depositing an oxide of silicon.

8. (Original) The process of Claim 7, wherein forming the second dielectric layer comprises chemical vapor deposition of a low-k material.

9. (Original) The process of Claim 7, wherein forming the second dielectric layer comprises spinning on a low-k material.

10. (Canceled)

11. (Withdrawn) A dielectric structure, comprising:

a plurality of posts disposed on a substrate, the posts comprising an electrically non-conductive material; and

a low-k dielectric material disposed around the posts.

12. (Withdrawn) The dielectric structure of Claim 11, wherein the substrate comprises a material selected from the group consisting of silicon carbide, silicon nitride, and carbon doped oxides of silicon.

13. (Withdrawn) The dielectric structure of Claim 11, wherein the posts are vertically oriented and comprised of an oxide of silicon.

14. (Withdrawn) The dielectric structure of Claim 13, wherein the oxide of silicon is a fluorine doped oxide.

15. (Withdrawn) The dielectric structure of Claim 13, wherein the posts have a rectangular base.

16. (Withdrawn) An integrated circuit, comprising:

a substrate having interconnected electrical elements therein;

a first dielectric layer disposed over the substrate;

at least one electrically non-conductive, vertically oriented post disposed on the first dielectric layer; and

a second dielectric layer disposed on the first dielectric layer such that the second dielectric surrounds the at least one post.

17. (Withdrawn) The integrated circuit of Claim 16, wherein the second dielectric layers has trenches therein.

18. (Withdrawn) The integrated circuit of Claim 17, further comprising metal disposed in the trenches.

19. (Withdrawn) The integrated circuit of Claim 18, wherein the metal comprises copper.

20. (Withdrawn) An integrated circuit, comprising:

a substrate having interconnected electrical elements therein;

a first dielectric layer disposed over the substrate;

a plurality of electrically insulating structures disposed on the first dielectric layer; and

a second dielectric layer disposed on the first dielectric layer such that the second dielectric surrounds the plurality of structures.

21. (Withdrawn) The integrated circuit of Claim 20,wherein the structures are identical.

22. (Withdrawn) The integrated circuit of Claim 20, further comprising metal filled damascene trenches in the second dielectric layer.

23. (Withdrawn) The integrated circuit of Claim 20, wherein the structures are comprised of an oxide of silicon, and the second dielectric layer is comprised of a porous material having a dielectric constant lower than that of silicon dioxide.

24. (Previously Presented) A process, comprising:

depositing a silicon nitride layer on a substrate;

depositing an insulating layer over the silicon nitride layer, wherein the insulating layer has a dielectric constant;

patterning the insulating layer such that a plurality of structures are formed, the structures each having a top surface;

depositing a porous dielectric material over and adjacent to the structures, the porous dielectric material having a void fraction, wherein the porous dielectric material substantially fills out the area adjacent to said structures and wherein the porous dielectric material has a dielectric constant, said dielectric constant of the insulating layer being higher than the dielectric constant of the porous dielectric material;

wherein said plurality of structures formed in the insulating layer provides mechanical reinforcement of the porous dielectric material which makes up the bulk of an inter-layer dielectric material;

polishing the porous dielectric material such that a top surface thereof is substantially even with the top surfaces of the structures; and

after polishing said porous dielectric material, forming an inlaid metal interconnection in the porous dielectric material.

25. (Withdrawn) The integrated circuit of Claim 24, wherein the porous dielectric material has a lower dielectric constant than that of the structures.

26. (Previously Presented) The process of Claim 24, further comprising treating the porous dielectric material such that its void fraction is increased.